Thermal Effect Reduction Layout Technique for Nano-Scale CMOS Technologies

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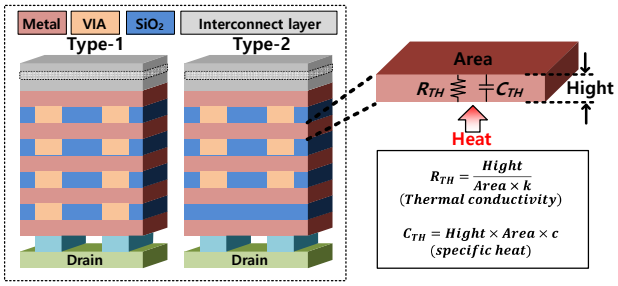
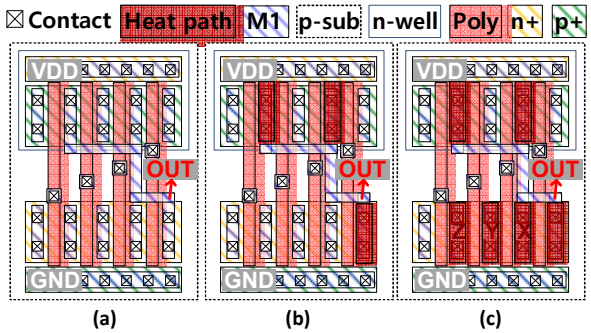
- **We propose a heat-path layout methodology to release heat confinement in Nano-Scale CMOS Technology.**
- **Since a conductive material-stack using metals and vias on the Si has trade-off relationship between junction temperature and circuit performance, we optimize the heat-path layout with different metal-stack floors with or without via1 and with different heat-path locations.**

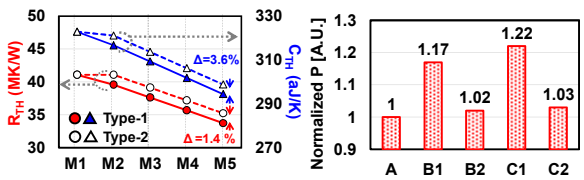
➢ Layout Technique



- **Two different types of heat-path and the calculation of R_{TH} and C_{TH} for each metal and via layers.**

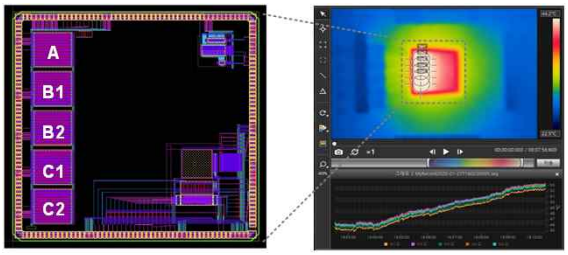


- **4-input NAND gate layout of (a) type-A, (b) type-B (B1: Using type-1, B2: Using type-2), (c) type-C (C1: Using type-1, C2: Using type-2).**



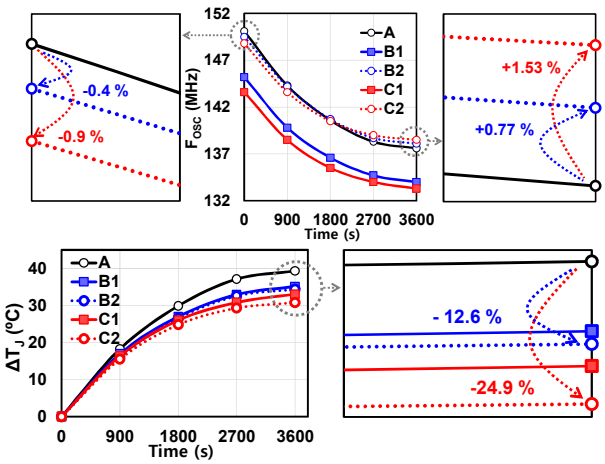
- **(a) R_{TH} and C_{TH} with the increase in metal stack-floors: type-1 and type-2.(b) Normalized power consumption of five types of ROs with different heat-paths**

➢ Measurement Environment



- **The photo of five types of R.O. layout for thermal imaging camera and chip photo.**
- **The manufactured chip can check temperature in real time with images and graphs through a thermal imaging camera.**

➢ Measurement Results



- **Due to the increase in C_p from the via1 of heat-path structure, B1 and C1 show a significantly lower f_{OSC}, compared to type-A.**
- **As a result, we prove type-2 (B2 and C2) is the thermal and power-efficient layout with the optimized heat-path.**

- **The measurement results of the ring oscillators with the proposed heat-path layout show 24.9% lower junction temperature and 1.53% increased oscillation frequency, compared to conventional layout.**
- **Since the proposed layout method shows the impact of optimized heat-path on the thermal effect for Nano-scale CMOS technology, we believe the proposed heat-path would be necessary for next-generation technologies of 5–7nm and beyond that suffer from the local thermal effect.**

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